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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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*Ex parte* ROSARIO GENNARO

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Appeal 2008-2944
Application 09/753,727
Technology Center 2400

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Decided:[1] May 7, 2009

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*Before* ALLEN R. MACDONALD, *Vice Chief Administrative Patent Judge,* ST. JOHN COURTENAY III, and DEBRA K. STEPHENS, *Administrative Patent Judges*.

STEPHENS, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

## STATEMENT OF THE CASE

Appellant appeals under 35 U.S.C. § 134(a) from a final rejection of claims 1-2, 6-7, 9-14, 18-19, 21-26, 30, 32, 34-37, 39-40, 44, and 47-52. Claims 3-5, 8, 15-17, 20, 27-29, 31, 33, 38, 41-43, and 45-46 have been cancelled.

We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM and introduce new grounds of rejection under 37 C.F.R. § 41.50(b).

### *Introduction*

According to Appellant, the invention is a structure and method for efficiently generating pseudo-random bits (Spec. 1, ll. 4-6).

### *Exemplary Claim(s)*

Claims 1 and 13 are exemplary claims and are reproduced below:

1. A computer program product for efficiently generating pseudo-random bits, the computer program product embodied on one or more computer readable media and comprising:

computer-readable program code means for providing an input value comprising C random bits;

computer-readable program code means for generating an output sequence comprising N pseudo-random bits using the provided C-bit input value as a short exponent x of a 1-way function G**x mod P that comprises

modular exponentiation modulo a safe N-bit prime number P, wherein a base G of the modular exponentiation is a fixed generator value;

computer-readable program code means for separating the N bits of the generated N-bit output sequence into a C-bit portion and an (N-C)-bit portion; and

computer-readable program code means for using the C-bit portion of the generated N-bit output sequence as the provided input value for a next iteration of the computer-readable program code means for generating while using the (N-C)-bit portion of the generated N-bit output sequence as pseudo-random output bits, until a desired number of pseudo-random output bits have been generated.

13. A system for efficiently generating pseudo-random bits in a computing environment, comprising:

means for providing an input value comprising C random bits;

means for generating an output sequence comprising N pseudo-random bits using the provided C-bit input value as a short exponent x of a 1-way function G**x mod P that comprises modular exponentiation modulo a safe N-bit prime number P, wherein a base G of the modular exponentiation is a fixed generator value;

means for separating the N bits of the generated N-bit output sequence into a C-bit portion and an (N-C)-bit portion; and

means for using the C-bit portion of the generated N-bit output sequence as the provided input value for a next iteration of the means for generating while using the (N-C)-bit portion of the generated N-bit output sequence as pseudo-random output bits, until a desired number of pseudo-random output bits have been generated.

*Prior Art*

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Schneier, Bruce, *Applied Cryptography*, John Wiley and Sons, 2nd ed., 225, 374-375 (1996).

Patel, Sarvar et al. *An Efficient Discrete Log Pseudo Random Generator*, Lecture Notes in Computer Science: Proceedings of the 18th Annual International Cryptology Conference on Advances in Cryptology, Springer-Verlag Berlin Heidelberg, 304-317 (1998).

*Rejections*

The Examiner rejected claim 52 as failing to comply with the written descriptions requirement under 35 U.S.C. § 112, first paragraph.

The Examiner rejected claim 52, under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Appellant regards as his/her invention.

The Examiner rejected claims 13-14, 18-19, 21-22, 24-26, 30, 32, 34-35, 37, 39-40, 44, 47, 49-52 as being anticipated under 35 U.S.C. § 102(b) by Patel.

The Examiner rejected claims 1-2, 6-7, 9-12, 23, 36, and 48 under 35 U.S.C. § 103(a) as being obvious over Patel and Schneier.

GROUPING OF CLAIMS

(1) Appellant argues claim 52 independently regarding the Examiner's rejection under 35 U.S.C. § 112, first paragraph for failing to comply with the written description requirement, the Examiner's rejection under 35 U.S.C. § 112, second paragraph for being indefinite, and the Examiner's rejection under 35 U.S.C. § 102(b) for anticipation by Patel.

(2) Appellant argues the rejection under 35 U.S.C. § 102(b) for anticipation by Patel of independent claims 13, 25, and 39 along with dependent claims 14, 18-19, 21-24, 26, 30, 32, 34-37, 40, 44, and 48-51 as a group on the basis of claim 13 (App. Br. 14 and 21). We will, therefore, treat claims 13, 14, 18-19, 21-26, 30, 32, 34-37, 39, 40, 44, and 48-51 as standing or falling with claim 13.

(3) Appellant argues the rejection under 35 U.S.C. § 103(a) as being obvious over Patel and Schneier of claims 1-2, 6-7, 9-12 and 48 as a group based on the arguments argued with respect to claims 13, 25, and 39 (App. Br. 23). We will, therefore, treat claims 1, 2, 6-7, 9-12, and 48 as standing or falling with claim 13.

We accept Appellant's grouping of the claims. See 37 C.F.R. § 41.37(c)(1)(vii) ("Notwithstanding any other provision of this paragraph, the failure of appellant to separately argue claims which appellant has grouped together shall constitute a waiver of any argument that the Board must consider the patentability of any grouped claim separately.")

## ISSUES

*Rejection under 35 U.S.C. § 112, first paragraph: Claim 52*

Appellant asserts the phrasing "ones of the bits" means "selected ones" or "particular ones" of the bits as opposed to the Examiner's interpretation which is that the bits are "ones" (not zeros) (Reply. 2-3 and Ans. 12-14).

*Issue:* Has Appellant met the burden of showing the Examiner erred in rejecting claim 52 under 35 U.S.C. § 112 first paragraph, as failing to comply with the written description requirement, for not disclosing in the Specification, an N-bit input value in which (N-C) uppermost contiguous *ones of the bits* are all set to zeros and in which C lowermost contiguous *ones of the bits* are random?

*Rejection under 35 U.S.C. § 112, second paragraph: Claim 52*

Appellant uses the term "effectively short" in claim 52 and indicates Appellant has no objection to deletion of "effectively short" (App. Br. 10, ¶ 23), a term the Examiner finds indefinite (Ans. 4).

*Issue:* Has Appellant met the burden of showing the Examiner erred in rejecting claim 52 for being indefinite due to use of the term "effectively-short"?

*Rejections under 35 U.S.C. §102(b):*

*Claim 52*

Appellant argues that Patel describes the lowermost bits are zero which is distinct from Appellant's invention of having the lowermost contiguous ones of the bits being random and the (N-C) uppermost bits being set to zero (App. Br. 12-13, ¶¶ 29-30). Appellant further argues Patel does not disclose how a generator functions but instead attempts to disprove the security of the generator (App. Br. 13, ¶ 30).

The Examiner contends Patel discloses the same generator as Appellant's invention, both of which have inputs in which the N-C uppermost bits are set to zero and the C lowermost bits are set to random (Ans. 15-17). The Examiner contends Patel discloses producing $x_i$ and the output of the generator is the trailing n-[c] bits of $x_i$ (Ans. 20). The Examiner therefore asserts Patel discloses outputting the (N-C) or n- $w$(log n) bit portion of the generated N-bit output sequence as pseudo-random output bits (Ans. 20).

*Issue:* Has Appellant met the burden of showing the Examiner erred in finding Patel discloses (N-C) uppermost bits are set to zero and the C lowermost bits are set to random in a pseudo-random number generator?

*Claims 1-2, 6-7, 9-14, 18-19, 21-26, 30, 32, 34-37, 39, 40, 44, and 47-51*

Appellant asserts their invention specifies an input value comprising C random bits provided as a short exponent x of a 1-way function G**x mod

P that generates an output sequence comprising N pseudo-random bits is not disclosed by Patel (App. Br. 14-15, ¶ 34). Appellant specifically asserts Patel's use of an N-bit exponent is a large exponent in contrast to Appellant's use of a short, C-bit exponent (App. Br. 15, ¶ 35). Appellant continues that Patel produces "n-c" bits per iteration and unlike Appellant's invention, repeatedly applies the extender to a random seed (App. Br. 16-17, ¶ ¶ 37-38). Appellant further argues Patel does not output a value that generates N pseudo-random bits using a short, C-bit exponent (App. Br. 19, ¶ 43). Appellant contends Patel describes using all N bits of the exponent in contrast to Appellant's invention (App. Br. 20, ¶ 44).

The Examiner finds Patel describes producing $x_i$ which consists of n bits and outputting n-*w*(log n) or N-C bits as random bits (Ans. 18). Further, the Examiner finds Patel discloses a "short exponent" generator that is the same iterative generator using the same mathematical function in the same way to generate the random bits as in Appellant's invention (*id.*). The Examiner further finds Patel does not disprove Patel is secure (Ans. 19). Moreover, the Examiner finds Patel generates a pseudo-random output and outputs N-C bits as random bits (Ans. 19-20). The Examiner finds Patel discloses a short exponent and although Patel may not recommend using this generator or the short exponent, Patel still had possession of and anticipated the generator and use of the short exponent (Ans. 20-21).

*Issue:* Has Appellant met the burden of showing the Examiner erred in finding Patel anticipates a generator using short exponents?

## FINDINGS OF FACT (FF)

*Appellant's Invention*

(1)In Appellant's pseudo-random bits generator, a seed length is "C" bits in length, where C < N and all successive inputs also use C-bit values (Spec. 16, ll. 10-11). Therefore, the top (N-C) bits of each iteration are set to all zeros (Spec. 16, l. 12). The generator iteratively computes x[i] = f([x-1]), but now only C bits are selected from the output N bits of each iteration as the value to be used for the next x; the remaining (N - C) bits are output as pseudorandom from each iteration (Spec. 16, ll. 14-17).

*Patel's Invention*

(2)Patel discloses a method and system for generating a discrete log pseudo random generator (Abstract). Discrete exponentiation modulo a prime *p* can hide *n-w*(log n) bits (*id.*). Information about the *n-w*(log n) bits can be used to discover the discrete log of $g^s$ mod p where *s* is a short exponent that has *w*(log *n*) bits (a constant *c* bits) (Abstract and pg. 307, § 2.1). The discrete logarithm with short exponents is used to produce a very efficient pseudo-random number generator which produces n-c bits per iteration (*id*).

(3)With appropriate selection of parameters, the discrete exponentiation function over a finite field, $g^{x_i} \bmod p$ is believed to be a one-way function (easy to compute but hard to invert) (pg. 304, § 1). A very

efficient cryptographic pseudo-random bit generator is attached to modular exponentiation in a finite field of cardinality $p$ where $p$ is a prime number of the form $2q + 1$ and $q$ is also prime (pg. 305-306, § 1). The generator generates n- *w (log n)* bits of every iteration which are simultaneously secure (pg. 306, § 1).

(4)A pseudo random bit generator produces n- *w (log n)* bits per iteration (pg. 313, ¶ 5). The new generator picks a seed $x_o$ from $Z_p^*$ and defines $x_{i+1} = g^{x_i} \bmod p$ (*id.*). At the $i^{th}$ step ($i > 0$), the new generator outputs the lower $n$-$w$ (log $n$) bits of $n$, except the least significant bit (*id.*).

(5)Patel discloses the discrete logarithm mod a prime p hides n- *w (log n)* bits by showing the simultaneous hardness of those bits (pg. 314, § 6). The hardness in this result is with respect to the discrete logarithm problem with short exponents (*id.*).

(6)Patel discusses some extensions of the results to be addressed in the future (pg. 315, § 7).

(7)The extension uses a secret seed, $x_0$, and defines $x_{i+1} = g^{x_i}$ iteratively (pg. 316, § 7.1). The output of the generator is the trailing $n$-$w$ (log $n$) bits of $x_i$, for all $i > 0$, where n = log $p$ (pg. 316, § 7.1).

(8)In another generator, *p, g,* and $x_0$ are used as the start but at each stage $x_{i+1} = g^{si}$ is defined where $s_i$ = leading $w$(log n) bits of $x_i$ (*id.*). This

ensures short exponents are used at each stage and hence, a significant speed up is guaranteed (*id.*).

## PRINCIPLES OF LAW

### *Claim Construction*

The Patent and Trademark Office (PTO) must consider all claim limitations when determining patentability of an invention over the prior art." *In re Lowry*, 32 F.3d 1579, 1582 (Fed. Cir. 1994) (citing *In re Gulack*, 703 F.2d 1381, 1385 (Fed. Cir. 1983)). "Claims must be read in view of the specification, of which they are a part." *Markman v. Westview Instruments, Inc.,* 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc).

"When the applicant states the meaning that the claim terms are intended to have, the claims are examined with that meaning, in order to achieve a complete exploration of the applicant's invention and its relation to the prior art." *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989). "[T]he specification is 'the single best guide to the meaning of a disputed term,' and that the specification 'acts as a dictionary when it expressly defines terms used in the claims or when it defines terms by implication." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1321 (Fed. Cir. 2005) (en banc) (citations omitted).

### *Anticipation*

A reference is anticipatory under § 102(b) when it satisfies particular

requirements. First, the reference must disclose each and every element of the claimed invention, whether it does so explicitly or inherently. *Eli Lilly & Co. v. Zenith Goldline Pharms., Inc.*, 471 F.3d 1369, 1375 (Fed. Cir. 2006). While those elements must be "arranged or combined in the same way as in the claim," *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1370 (Fed. Cir. 2008), the reference need not satisfy an ipsissimis verbis test, *In re Bond*, 910 F.2d 831, 832–33 (Fed. Cir. 1990). Second, the reference must "enable one of ordinary skill in the art to make the invention without undue experimentation." *Impax Labs., Inc. v. Aventis Pharms. Inc.*, 545 F.3d 1312, 1314 (Fed. Cir. 2008); *see In re LeGrice*, 301 F.2d 929, 940–44 (CCPA 1962). As long as the reference discloses all of the claim limitations and enables the "subject matter that falls within the scope of the claims at issue," the reference anticipates—no "actual creation or reduction to practice" is required. *Schering Corp. v. Geneva Pharms., Inc.*, 339 F.3d 1373, 1380–81 (Fed. Cir. 2003); *see In re Donohue*, 766 F.2d 531, 533 (Fed. Cir. 1985). This is so despite the fact that the description provided in the anticipating reference might not otherwise entitle its author to a patent. *See Vas-Cath Inc. v. Mahurkar,* 935 F.2d 1555, 1562 (Fed. Cir. 1991) (discussing the "distinction between a written description adequate to support a claim under § 112 and a written description sufficient to *anticipate* its subject matter under § 102(b)").

*Obviousness*

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). *See also In re Piasecki*, 745 F.2d 1468, 1472 (Fed. Cir. 1984). Only if this initial burden is met does the burden of coming forward with evidence or argument shifts to the Appellant. *Oetiker*, 977 F.2d at 1445. *See also Piasecki*, 745 F.2d at 1472.

Appellant may sustain this burden by showing that the Examiner failed to provide sufficient evidence to show that one having ordinary skill in the art would have done what Appellant did. *United States v. Adams*, 383 U.S. 39 (1966); *In re Kahn*, 441 F.3d 977, 987-88 (Fed. Cir. 2006); *DyStar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick, Co.*, 464 F.3d 1356, 1360-61 (Fed. Cir. 2006).

ANALYSIS

*35 U.S.C. § 112, first paragraph: Claim 52*

Claim 52 recites uppermost contiguous ones of the bits are set to zero and the lowermost contiguous bits are random. The Examiner has interpreted the claim language to mean that in the uppermost bits, contiguous ones in those uppermost bits are set to zero (Ans. 13). Appellant argues the claim language should be interpreted as setting the top contiguous bits to zero (App. Br. 2-3, ¶¶ 2b. – 2c.).

The Examiner agrees antecedent bases exist for the limitation of the top (N-C) bits being set to zero while the remaining C bits are random (Ans. 3-4). Therefore, based on this finding by the Examiner, we find Appellant has stated the meaning that the claim terms are intended to have (FF 1 and App. Br. 8-9). Accordingly, we conclude the meanings of the claim terms set forth by Appellant have been clearly defined and therefore, that Appellant has met the burden of showing the Examiner erred in finding the element including an N-bit input value in which (N-C) uppermost contiguous *ones of the bits* are all set to zeros and in which C lowermost contiguous *ones of the bits* are random lacks a written description.

*Rejection under 35 U.S.C. § 112, second paragraph: Claim 52*

Appellant has not presented any arguments regarding this rejection but instead agree to remove the term "effectively short" in claim 52. Thus, since Appellant has presented no arguments, we conclude the Examiner has not erred in rejecting claim 52 for being indefinite due to use of the term "effectively-short".

*35 U.S.C. § 102(b): Claim 52*

Patel discloses a pseudo random generator that Patel indicates merits further exploration (FF 6). Patel describes this generator specifically stating that short exponents are used (FF 7). The output of the generator is the trailing $n$-$w$ (log $n$) bits of $x_i$ (FF 7); therefore, n-c bits are output and the

remaining c-bits (or the leading $w$(log n) bits) of the previous iteration are used as the short exponent input to the generator (FF 8).

We also find, based on the Examiner's reasons (Ans. 16), that all of the place values greater than the Cth place value of the number are inherently set to zero and the c lowermost bits are random according to the generator (FF 8).

Appellant additionally argues Section 7 does not anticipate Appellant's invention because it discusses extensions of Patel's work that will be addressed in the future (FF6). We find Patel, including this section, discloses each and every element of the claimed invention as required for anticipation. Additionally, we conclude this section enables the subject matter that falls within the scope of the Appellant's claims.

Accordingly, we find Appellant has not shown the Examiner erred in finding Patel discloses (N-C) uppermost bits are set to zero and the C lowermost bits are set to random in a pseudo-random number generator using a short exponent. Therefore, we sustain the Examiner's rejection of claim 52 as being anticipated by Patel under 35 U.S.C. § 102(b).

*35 U.S.C. § 102(b) and § 103(a):*

*Claims 1-2, 6-7, 9-14, 18-19, 21-26, 30, 32, 34-37, 39, 40, 44, and 47-51*

Patel discloses use of a short exponent to increase the speed of the generator (FF 8). For this generator, the output of the generator is the trailing $n$-$w$ (log $n$) bits of $x_i$, for all $i > 0$, where n = log $p$ (FF 7). Patel

defines c = $w$ (log $n$); therefore, we find Patel discloses a short exponent pseudo random number generator that outputs n-c bits.

Appellant argues since Patel indicates these are extensions that will be reviewed further and since Patel questions if the security of the generator will be impacted by use of a short exponent, Patel did not have possession of the invention (Reply 6-7, ¶¶ 4a.–4b.).

We find Section 7 Appendix of Patel, including § 7.1, discloses each and every element of the claimed invention. Additionally, we conclude this Section enables the subject matter that falls within the scope of the Appellant's claims. Although Patel indicates that the extensions of the results will be addressed in the future (FF 6), we find Patel describes the generator in sufficient detail as to describe each and every element of the claimed invention. Patel sets out several questions that will need to be answered, i.e., "Will this speed impact the security of the generator?" (pg. 316, § 7.1), this question is directed toward the results of the extension (the generator). Therefore, this question and the other unanswered questions in that section are not relevant as to whether the reference anticipates Appellant's invention as claimed.

Therefore, after considering the totality of the record before us, we conclude Appellant has not met the burden of showing the Examiner erred in finding Patel discloses a generator that uses short exponents and outputs n-c bits.

We affirm the Examiner's rejection of independent claims 13, 25, and 29 for anticipation by Patel. Since claims 14, 18-19, 21-22, 24, and 49 depend directly from independent claim 13; claims 26, 30, 32, 34-35, 37, and 50 depend directly from claim 25; and claims 40, 44, 47, and 51 depend from claim 39, and these claims were not separately argued, we affirm the Examiner's rejections of claims 13-14, 18-19, 21-22, 24, 26, 30, 32, 34-35, 37, 39-40, 44, 47, 49, and 51 for anticipation by Patel. Additionally, since claims 1-2, 6-7, 9-12, 23, 36, 48 and 50 were not separately argued, we affirm the Examiner's rejection for obviousness over Patel and Schneier.

## CONCLUSION

Based on the findings of facts and analysis above, we find Appellant has sufficiently conveyed with reasonable clarity to those skilled in the art that Appellant was in possession of the invention as of the filing date (i.e., the N-bit input value in which (N-C) uppermost contiguous *ones of the bits* are all set to zeros and in which C lowermost contiguous *ones of the bits* are random; *see* claim 52). Accordingly, we find Appellants have met the burden of showing error in the Examiner's proffered prima facie case under the written description requirement of 35 U.S.C. § 112, first paragraph.

We additionally conclude Appellant has not met the burden of showing the Examiner erred in rejecting claim 52 for being indefinite due to use of the term "effectively-short".

Further, we conclude Appellant has not met the burden of showing the Examiner erred in finding Patel discloses (N-C) uppermost bits are set to zero and the C lowermost bits are set to random in a pseudo-random number generator.

Lastly, we conclude Appellant has not met the burden of showing the Examiner erred in finding Patel discloses a generator that uses short exponents and outputs n-c bits and that Patel had possession of and anticipated a generator using short exponents.

## NEW GROUNDS OF REJECTION

### *35 U.S.C. § 101:*

### *Claims 25-26, 30, 32, 34-37, 50, and 52*

Claims 25-26, 30, 32, 34-37, 50, and 52 recite methods. The Court of Appeals for the Federal Circuit, in the *In re Bilski* decision, clarified the bounds of patent-eligible subject matter for process claims. *See In re Bilski*, 545 F.3d 943 (Fed. Cir. 2008) (en banc). The *Bilski* court found "the machine-or-transformation test, properly applied, is the governing test for determining patent eligibility of a process under § 101." *See Bilski* at 956.

The *Bilski* court, in following the Supreme Court, enunciated the machine-or-transformation test as follows: "A claimed process is surely patent-eligible under § 101 if: (1) it is tied to a particular machine or apparatus, or (2) it transforms a particular article into a different state or thing." *Id.* at 954 (citing Benson, 409 U.S. at 70 (1972)).

None of these claims recite a particular machine or apparatus. None of the claims transform a particular article into a different state or thing. All of the claims recite mathematical algorithms. Thus, we conclude the claims do not recite statutory matter and therefore reject claims 25-26, 30, 32, 34-37, 50, and 52 under 35 U.S.C. § 101.

## DECISION

The Examiner's rejection of claim 52 under 35 U.S.C. § 112, first paragraph for failing to comply with the written description requirement is reversed.

The Examiner's rejection of claim 52 under 35 U.S.C. § 112, second paragraph for being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention is affirmed.

The Examiner's rejection of claim 52 under 35 U.S.C. § 102(b) for anticipation by Patel is affirmed.

The Examiner's rejection of claims 13-14, 18-19, 21-22, 24-26, 30, 32, 34-35, 37, 39-40, 44, 47, and 49-52 as being anticipated under 35 U.S.C. § 102(b) by Patel is affirmed.

The Examiner's rejection of claims 1-2, 6-7, 9-12, 23, 36, and 48 under 35 U.S.C. § 103(a) as being obvious over Patel and Schneier is affirmed.

We have affirmed at least one rejection of each claim; therefore, we affirm the Examiner's rejection of the claims on appeal.

In addition to affirming the Examiner's rejections, this decision contains a new ground of rejection pursuant to 37 C.F.R. § 41.50(b), rejection of claims 25-26, 30, 32, 34-37, 50, and 52 for reciting non-statutory matter under 35 U.S.C. § 101. 37 C.F.R. § 41.50(b) provides that "[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review."

37 C.F.R. § 41.50(b) also provides that the Appellant, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:

> (1) Reopen prosecution. Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner....
>
> (2) Request rehearing. Request that the proceeding be reheard under § 41.52 by the Board upon the same record....

Should Appellant elects to prosecute further before the Examiner pursuant to 37 C.F.R. § 41.50(b)(1), in order to preserve the right to seek review under 35 U.S.C. §§ 141 or 145 with respect to the affirmed rejection, the effective date of the affirmance is deferred until conclusion of the prosecution before the Examiner unless, as a mere incident to the limited

prosecution, the affirmed rejection is overcome.

If Appellant elects prosecution before the Examiner and this does not result in allowance of the application, abandonment or a second appeal, this case should be returned to the Board of Patent Appeals and Interferences for final action on the affirmed rejection, including any timely request for rehearing thereof.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED
37 C.F.R. § 41.50(b)

rwk

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